Adaptive Digital Slope Compensation for Peak Current Mode Control

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Abstract— **Peak current mode control as well as digital control offers a number of benefits. Therefore it is an interesting approach to combine these two techniques in one control structure. Based on microcontrollers with on-chip comparators, this combination is realizable with very low effort. In order to eliminate the drawbacks of peak current mode control, a slope compensation has to be added. This paper presents such a slope compensation implemented on a microcontroller not using an analog ramp signal but instead pre-calculating the desired comparator switch-off threshold. In contrast to conventional analog control, adaptive algorithms can be used to maintain optimal slope compensation over a wide operating range. Problems that occur in practice due to reverse recovery current spike and computing time can be handled with simple measures. The effectiveness of the proposed digital slope compensation is verified by experimental results.**

Index Terms— **Digital slope compensation, digital control, peak current mode control, switched-mode power supplies.**

I. INTRODUCTION

Current mode control is the commonly used control method for switched-mode power supplies (SMPS). Compared to voltage mode control, it exhibits a high frequency bandwidth resulting in improved control loop dynamics and leads to a better line noise rejection. With reducing the small-signal dynamics from second-order to first-order, it additionally simplifies the outer voltage loop design [1-2].

Current mode control can be classified into average current mode and peak current mode. As the name implies, average current mode control adjusts the average inductor current. In particular, in boost-type power factor correction (PFC) rectifiers, average current control ensures very low current distortions [8]. Peak current mode is the widely-used current mode control technique, where the duty cycle is terminated when the inductor current reaches a threshold level defined by the outer voltage controller. This technique features some inherent advantages such as simple cycle-by-cycle current limiting and good current sharing of paralleled converters [1-2]. A combination of average and peak current control is the transition or boundary mode control, where the converter is driven at the border of continuous (CCM) and discontinuous conduction mode (DCM). Characteristic of the boundary mode is the varying switching frequency and that the peak current is twice as
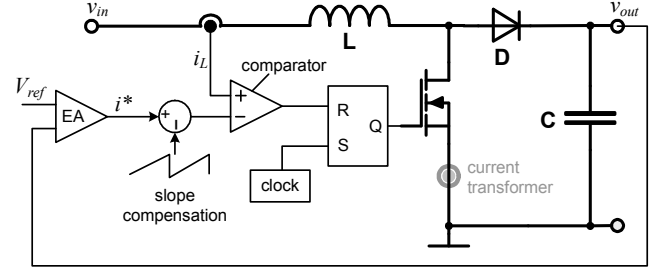

Fig. 1. Peak current controlled boost converter with slope compensation

large as the average current. But extra effort is needed to detect the zero current.

However, there are several drawbacks of peak current mode control in CCM [3-4]: The control is loosing stability, if the duty cycle exceeds 50 %, resulting in subharmonic oscillations, non ideal control response caused by peak instead of average current sensing and noise sensitivity, particularly at small inductor current ripple.

A common approach to regain stability is to apply a so-called slope compensation in peak current controlled converters with duty cycles above 50 % [1-7].

With increasing computing capability and decreasing cost, DSP and microcontroller-based digital control becomes increasingly important in SMPS applications [8-10]. This measure offers a number of benefits such as flexibility and programmability, decreased number of active and passive components resulting in improved reliability, negligible or compensable offsets and thermal drifts. Additionally, digital control offers the potential of implementing sophisticated, adaptive and nonlinear control methods to improve static and dynamic performance.

Completely digitally controlled converters predominantly calculate the duty cycle and use integrated digital pulse width modulation (DPWM) generators to control the switches [9]. Also the full digital peak current control presented in [8] is based on pre-calculating the desired duty cycle requiring accurate knowledge of the inductor value L. Using these techniques, the inherent advantages of peak current control mentioned above could not be used.

However, with available microcontrollers including on-chip comparators and dedicated DACs at the internal input, a purely digital peak current control is basically feasible with a simple component. Nevertheless, the implementation

of the slope compensation in a digital control stays challenging, since a continuously increasing ramp function is needed during each switching cycle.

In this contribution, a digital slope compensation technique for peak current control is proposed not using a ramp, but rather pre-calculating the desired comparator switch-off threshold depending on the valley inductor current. Knowledge of the inductor value L is not necessary. Adaptive algorithms keep the amount of slope compensation adjustable to achieve minimum response time without occurrence of subharmonic oscillation.

The paper is structured as follows. Basics of peak current control with slope compensation are reviewed in Section II. In Section III the *digital* slope compensation technique is derived and is verified via simulation in Section IV. The practical implementation and measurement results are given in Section V.

II. PEAK CURRENT MODE WITH SLOPE COMPENSATION

Current mode control is subject of numerous publications, for example [1, 11-12]. The control blocks of a boost converter with outer voltage loop and inner peak current control loop with analog slope compensation is shown in Fig. 1. The basic principles of peak current mode control and the need of a slope compensation are referred to in this section.

A. Situation without Slope Compensation

In order to derive the stability criterion of peak current mode controlled CCM converters which characterizes the transition to subharmonic oscillations, the operation without slope compensation shall be analyzed in a first step. Therefore we refer to Fig. 2 where an undisturbed (solid stroke) and a disturbed (dashed stroke) inductor current are plotted versus a single switching period T_s. Both inductor current shapes have the same rising slope m_1, falling slope m_2 and peak value $\hat{i}$.

For the *undisturbed* case (solid line in Fig. 2) it can be directly derived

$$\hat{i} = m_1 \cdot T_1 + I_0 \tag{1}$$

as well as

$$\hat{i} - m_2 \cdot T_2 = I_0. \tag{2}$$

Whereas for a *disturbance* of Δi_0 (dashed line in Fig. 2)

$$\hat{i} = \Delta i_0 + m_1 \cdot T_{1d} + I_0 \tag{3}$$

and

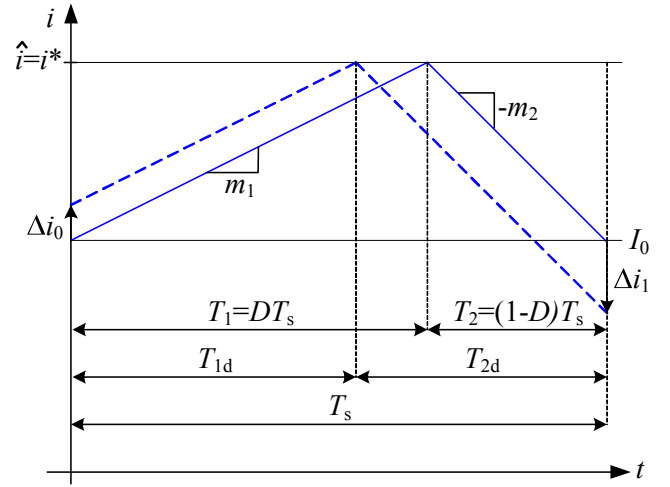$$\hat{i} - m_2 \cdot T_{2d} = I_0 + \Delta i_1 \tag{4}$$

applies.

Fig. 2. Growing disturbances in the inductor current under peak current control for $m_2 > m_1$

In both cases the duration of the switching period is identical, because of time-triggered turn-on,

$$T_s = T_1 + T_2 = T_{1d} + T_{2d}. \tag{5a}$$

After solving (1) for T_1, (2) for T_2, (3) for T_{1d} and (4) for T_{2d} equation (5a) can be rewritten as

$$\frac{\hat{i} - I_0}{m_1} + \frac{\hat{i} - I_0}{m_2} = \frac{\hat{i} - \Delta i_0 - I_0}{m_1} + \frac{\hat{i} - \Delta i_1 - I_0}{m_2} \tag{5b}$$

and directly simplified to

$$0 = -\frac{\Delta i_0}{m_1} - \frac{\Delta i_1}{m_2}, \tag{5c}$$

which is equivalent to

$$\Delta i_1 = -\frac{m_2}{m_1} \cdot \Delta i_0. \tag{5d}$$

If the magnitude of the current falling slope m_2 is larger than that of the rising slope $m_1 < m_2$ the current perturbation Δi obviously grows. The current error drift propagates with every switching period and after n cycles the perturbation will become

$$\Delta i_n = \left(-\frac{m_2}{m_1}\right)^n \cdot \Delta i_0. \tag{6}$$

For *steady state* conditions the ratio of current falling slope to rising slope can be expressed as

$$\frac{m_2}{m_1} = \frac{D}{1-D} \tag{7}$$

where D is the duty cycle (c.f. also Fig. 3).

From (6) and (7) it follows that the instability inherently occurs as long as the duty cycles exceed 50 % ($D > 0.5$).
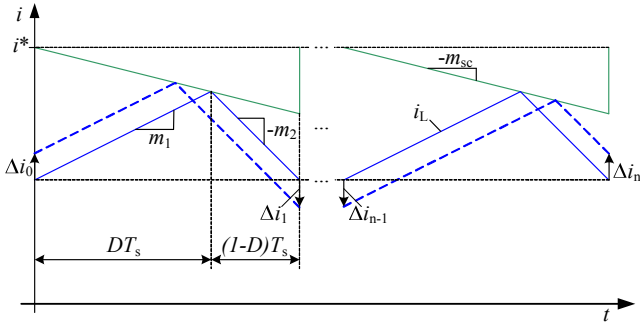
Fig. 3. Inductor current under peak current control with slope compensation

B. Situation with Slope Compensation

The instability for $D > 0.5$ can be eliminated, if a compensation ramp is added to the switch-off threshold as shown in Fig. 3 [1-7]. When introducing the additional compensation slope m_{sc} the calculation similar to (1)-(6) directly yields as modified formula for the current perturbation after n cycles

$$\Delta i_n = \left(-\frac{m_2 - m_{sc}}{m_1 + m_{sc}} \right)^n \Delta i_0. \tag{8}$$

From (8) it follows that for a stable current loop $\left| \frac{m_2 - m_{sc}}{m_1 + m_{sc}} \right| < 1$ must be fulfilled and therefore the required amount of compensation ramp results as

$$m_{sc} > \frac{1}{2}(m_2 - m_1). \tag{9}$$

Assuming a constant inductance L, the slope is proportional to the inductor voltage. Table I contains the corresponding voltages $m_1 L$, $m_2 L$ and the required compensation $m_{sc}L$ for buck, boost and buck-boost converter.

TABLE I
CURRENT SLOPE GENERATING VOLTAGES AND MINIMUM REQUIRED COMPENSATION FOR BASIC CONVERTERS

	$m_1 L$	$m_2 L$	$m_{sc} L$
Buck	$V_{in} - V_{out}$	V_{out}	$> V_{out} - 0.5 V_{in}$
Boost	V_{in}	$V_{out} - V_{in}$	$> 0.5 V_{out} - V_{in}$
Buck-Boost	V_{in}	V_{out}	$> 0.5(V_{out} - V_{in})$

From (8) it can be seen that a perturbation can be compensated within only one cycle, if the slope of the compensation ramp m_{sc} is equal to the falling current slope m_2. This characteristic is called *dead-beat* control and represents the fastest possible transient response [1-6]. In the following this condition is named optimum slope compensation. If applying higher values of m_{sc} than m_2, the settling takes several cycles without overshoot.

In applications with relatively small variation in input and output voltages, resulting in nearly constant duty cycle, a constant compensation slope suffices to achieve optimum compensation. Under varying input or output voltage (e.g. with PFC applications), the magnitude of the required compensation slope varies dynamically. Various solutions are known, for example adaptive slope compensation [6], piecewise linear slope compensation [3] and as widely used nonlinear slope compensation [2]. These techniques provide on the one hand optimum slope compensation over a wide range of duty cycle, but on the other hand they require more or less complex additional circuitry. Furthermore, using passive components provides no flexibility and inaccuracies caused by component tolerance and thermal drift are likely to occur.

III. DIGITAL SLOPE COMPENSATION

All slope compensation techniques described in the previous section base on analog circuitry implementations. With the impact of digital control in SMPS it is desirable also to implement peak current control in a digital manner. This is feasible with microcontrollers containing analog comparators (e.g. PIC, dsPIC, Piccolo). Thereby the discrete threshold value is converted into an analog voltage representing the current threshold level for the on-chip comparator. The DPWM unit is used to turn on at the beginning of each new cycle and to limit the duty cycle to a maximum tolerable value. The comparator output is directly linked with DPWM generator and forces the DPWM output to turn off. Because no current has to be sampled and no code has to be executed to compute a duty cycle the introduced deadtime is minimized for the current control loop.

However, with the need of slope compensation an adequate technique for this digital peak current control has to be designed. An obvious solution could be to remain the slope compensation in analog technique and add a ramp to the inductor current signal. Using such an approach, however, no benefits in terms of complexity and adaptivity can be achieved. Digital implementation of the ramp compensation requires to permanently decrement the discrete threshold value within every switching cycle with minimal possible step size. This appears to be impractically using a reasonable microcontroller.

Hence, the task arises to propose a concept of digital slope compensation without using a ramp. Instead, the desired threshold level with integrated amount of compensation is pre-calculated by means of the valley current i_n, i.e. the inductor current i_{L_min} at the beginning of the cycle n. As indicated in Fig. 4, the current threshold level i_{cmp} can be expressed as

$$i_{cmp} = i_n + m_1 \cdot DT_s \tag{10}$$

or

$$i_{cmp} = i^* - m_{sc} \cdot DT_s. \tag{11}$$

From (10) and (11) we obtain

$$DT_s = \frac{i^* - i_n}{m_1 + m_{sc}} \cdot \qquad (12)$$

Using (12) to eliminate DT_s from (11) we get

$$i_{cmp} = i^* - m_{sc} \frac{i^* - i_n}{m_1 + m_{sc}} \cdot \qquad (13)$$

At this point we introduce a compensation factor k_{sc} as

$$k_{sc} = \frac{m_{sc}}{m_1} \cdot \qquad (14)$$

Thus (13) can be expressed as

$$i_{cmp} = i^* - \frac{k_{sc}}{1 + k_{sc}}\left(i^* - i_n\right) \text{ or } i_{cmp} = \frac{1}{1 + k_{sc}}\left(i^* + k_{sc} i_n\right) \cdot \qquad (15)$$

Hence, the required current threshold level for the comparator can be computed by the current reference value i^* and the valley current value i_n. The current reference i^* is obtained from the voltage controller and the valley current i_n has to be sampled every switching-on event and passed via analog-digital converter (ADC) to the digital control.
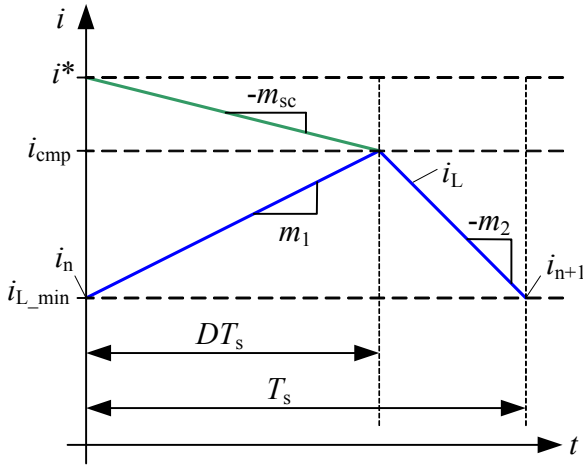

Fig. 4. Inductor current characteristics to illustrate principle of digital slope compensation

In order to fit the computed threshold value with adequate slope compensation, a proper value for the compensation factor k_{sc} has to be chosen. The minimum desired values to avoid subharmonic oscillations and values for optimum slope compensation for buck, boost and buck-boost converter extracted from Table I are summarized in Table II. Note, that the minimum value for k_{sc} needs to be limited to zero.

By measuring input and output voltage it is quite simple to use the entries from Table II to implement an algorithm for an adaptive compensation factor that guarantees desired dynamic over a wide range of operation.

The structure of the digital control is illustrated in Fig. 5.

Computation of an adaptive compensation factor is an option and can be replaced by a constant value if no adaptivity is required. It has to be pointed out, that no knowledge of inductor value or other circuit parameters is required for the proposed current control technique.

TABLE II
COMPENSATION FACTOR FOR MINIMUM REQUIRED AND OPTIMUM SLOPE COMPENSATION FOR BASIC CONVERTERS

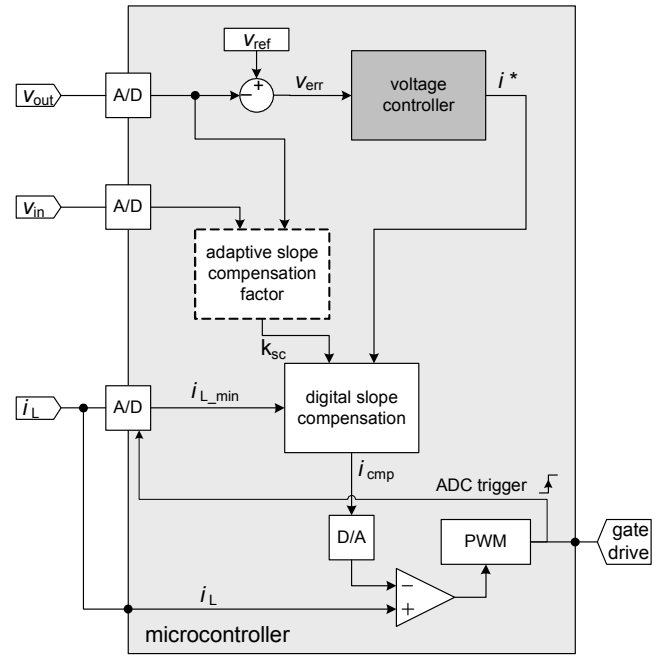|	min. k_{sc}	optimum k_{sc}
Buck	$\dfrac{V_{out} - 0.5 V_{in}}{V_{in} - V_{out}}$	$\dfrac{V_{out}}{V_{in} - V_{out}}$
Boost	$\dfrac{0.5 V_{out} - V_{in}}{V_{in}}$	$\dfrac{V_{out} - V_{in}}{V_{in}}$
Buck-Boost	$\dfrac{0.5\left(V_{out} - V_{in}\right)}{V_{in}}$	$\dfrac{V_{out}}{V_{in}}$

Fig. 5. Scheme of the digital control structure implemented on microcontroller

Assuming inductor currents of triangular shape it is possible to identify the average inductor current i_{avg} with the known current extrema i_{cmp} and i_n:

$$i_{avg} = \frac{1}{2}\left(i_{cmp} + i_n\right) \qquad (16)$$

This can be useful in PFC applications to maintain sinusoidal input current.

IV. SIMULATION RESULTS

First, the effectivity of the digital slope compensation concept is verified by simulation. Therefore this method is compared with the equivalent conventional slope compensation.
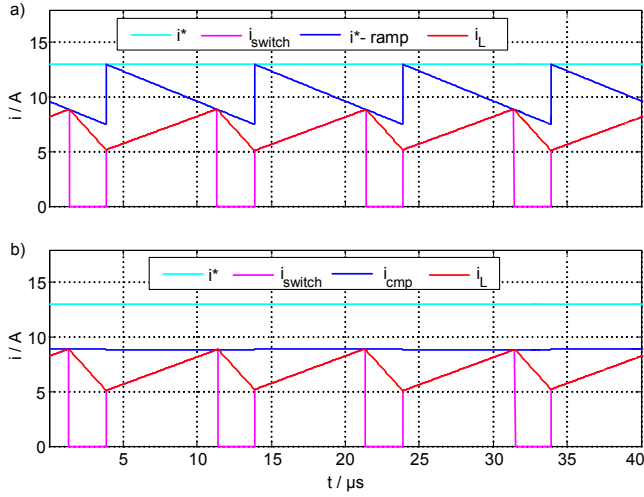
Fig. 6 Simulation results of peak current control with slope compensation under steady state conditions ($D = 0.82$, $k_{sc} = 1.8$)
a) with conventional compensation ramp
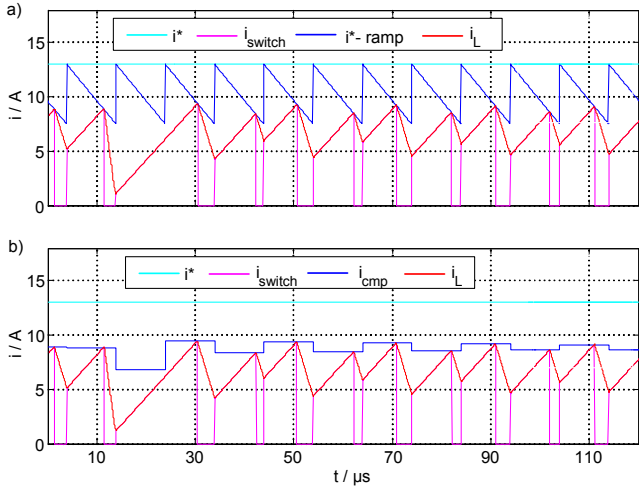b) with computed current threshold level

Fig. 7. Simulation results with perturbed inductor current
a) with conventional compensation ramp
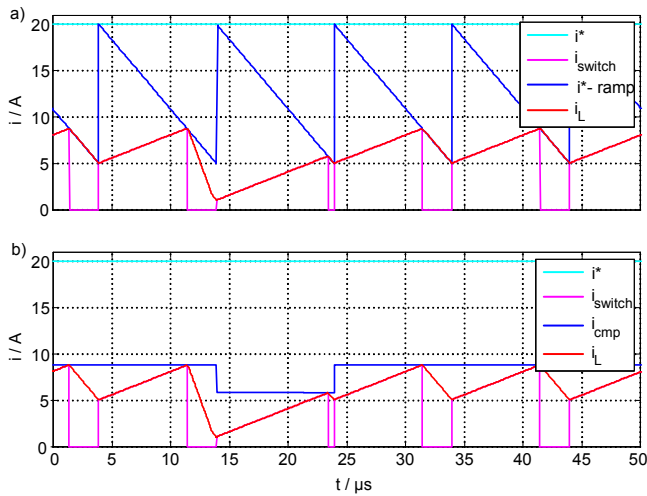b) with computed current threshold level

Fig. 8. Simulation results with perturbed inductor current and optimum k_{sc} value
a) with conventional compensation ramp
b) with computed current threshold level

Fig. 6 shows the inductor current under steady state conditions with conventional compensation ramp and with digital slope compensation. As can be seen, there is no difference in the resulting current shapes.

Fig. 7 and Fig. 8 illustrate the response of the peak current control to a simulated perturbation in the inductor current. In Fig. 7 a small compensation factor close to the minimum required compensation was used, so that settling of the inductor current takes several cycles. When applying the optimum slope compensation, the settling of the inductor current occurs within one cycle, as shown Fig. 8.

V. PRACTICAL IMPLEMENTATION AND MEASUREMENT RESULTS

After extensive simulations, the control structure depicted in Fig. 5 was implemented on a 16 bit microcontroller with on-chip comparators (Microchip dsPIC30F2020). This platform was used to control a simple boost converter forming the PFC rectifier stage of a standard industrial AC-DC converter (cf. Fig. 9). In order to test the practical feasibility of the digital slope compensation concept the power supply was powered with DC input voltage.

Fig. 9. Modified AC-DC converter system of 2 kW containing the boost converter

Compared to simulation there are mainly two challenges occurring in practice. The first problem turns up if the current is measured in the MOSFET path like indicated pale in Fig. 1. This is the case if a simple current transformer is used as sensor. Because of the reverse recovery effect of the boost diode, a current spike appears in the MOSFET path at the beginning of each new cycle (cf. Fig. 10). If current measurement is done in this path, the minimum inductor current cannot be sampled instantaneously at turn-on. However, with a short delay of approximately 600 ns, after the reverse recovery process is completed, the current value can be used. Another problem also caused by the reverse recovery current is that a high current spike can exceed the comparator turn-off threshold and force a faulty trigger of the comparator. This leads to erratic subharmonic oscillations as indicated in Fig. 11.

Therefore a leading edge blanking was implemented in software by deactivating the comparator during the reverse recovery process.
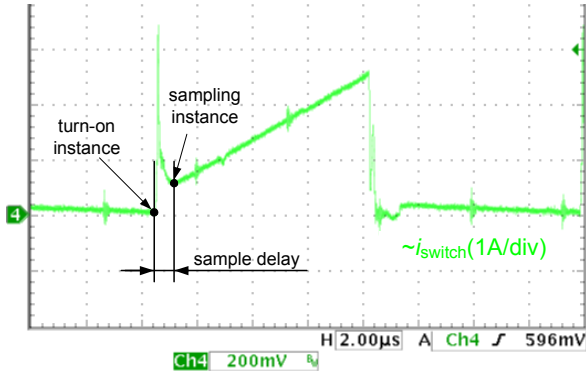

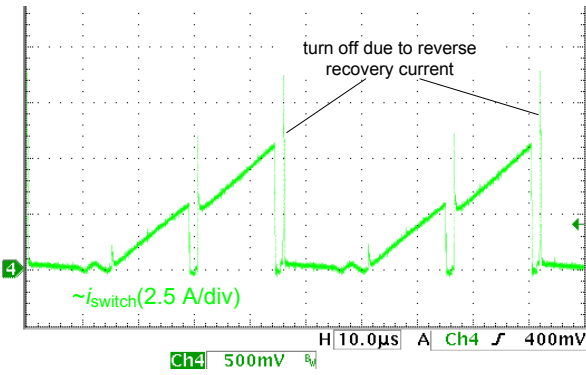Fig. 10. Switch current with current spike and sampling instance

Fig 11. Subharmonic oscillation due to faulty activation at reverse recovery current spike

The second difference to simulation is the delay due to the computing time. If the current reaches the old threshold value calculated in the previous cycle before the new threshold value is updated, a premature turn-off occurs. This can also result in undesired subharmonic oscillation (cf. Fig. 12). To avoid such unmeant trigger of the comparator, the threshold value is set to the maximum value before each cycle until the computation of the new threshold value is finished. In order to minimize the resulting dead time, the comparator threshold value is computed firstly in the interrupt routine. Thus, the threshold value is computed with the k_{sc} value of the previous cycle. However, this is not essential as k_{sc} only depends on the relative slowly varying voltage values (cf. Table II).

Considering the mentioned practical aspects, the timing shown in Fig. 13 follows. With this implementation, the control loop operates up to high duty cycle values (cf. Fig. 14) without subharmonic oscillation.

The transient response of a current reference step with an implemented slope factor slightly above the minimum required value is shown in Fig. 15 for a step-up and in Fig. 16 for a step-down. This confirms the high dynamic performance and robustness of the peak current control

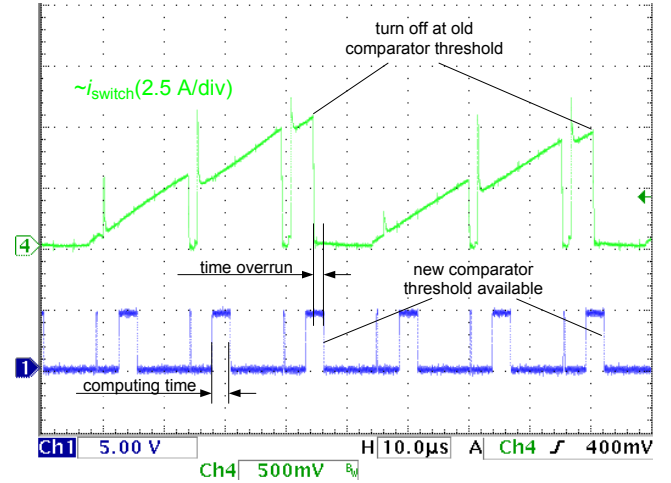method with applied digital slope compensation.

Fig. 12. Subharmonic oscillation due to turn off at comparator threshold value of previous cycle
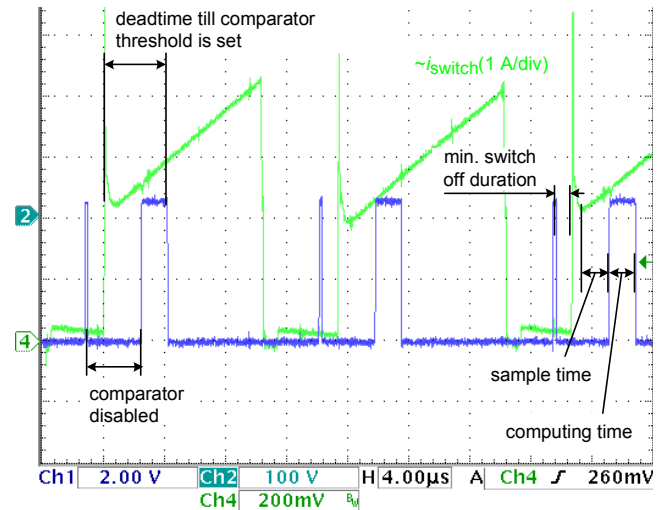

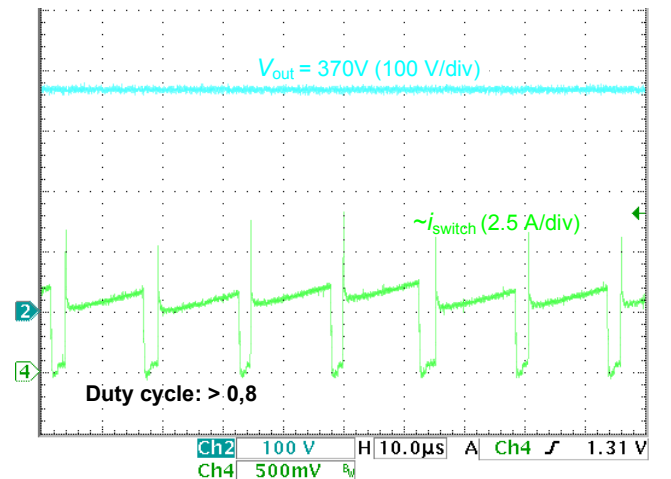Fig. 13. Time flow within the switching cycles

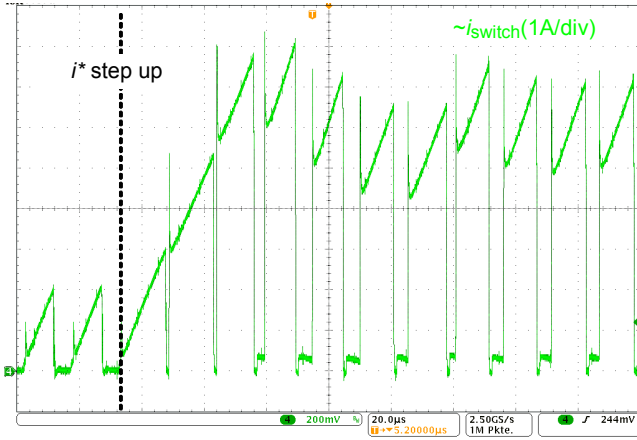Fig. 14. Shape of current at high duty cycle

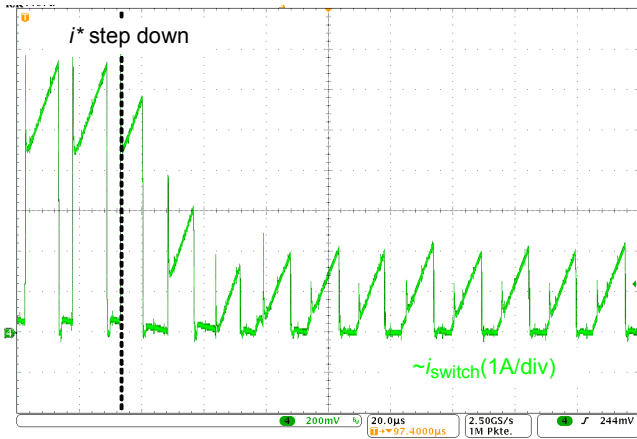Fig. 15. Transient response for a step-up current reference

Fig. 16. Transient response for a step-down current reference

VI. CONCLUSIONS

Up to now peak current control was predominantly implemented in technique of analog circuitry. However, by dint of available microcontroller with on-chip comparators digital peak current control is feasible with little effort.

The need of slope compensation at duty cycles above 50 % to avoid subharmonic oscillation can be solved with simple, but effective digital algorithms. Therefore, it suffices to sample only the valley inductor current. Knowledge of the inductance or any other specific values is superfluous. By directly triggering the PWM unit via on-chip comparator only little computing power is required, whereby the current control can be processed by a simple microcontroller superseding a costly DSP.

Problems occurring in practice due to the reverse recovery current spike and the computing time can be handled with simple measures. So the digital slope compensation turns out as a practical alternative in peak current controlled applications.

Furthermore, a digital implementation offers the potential to apply adaptive slope compensation. Thus, the amount of slope compensation can be adjusted depending on the input and output voltage relation of the converter. This guarantees requested dynamic performance of the current control loop from dead beat up to a desired settling time with or without overshoot.

VII. REFERENCES

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