Improved PLL structures for single-phase grid inverters

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***Abstract* — Phase, amplitude and frequency of the utility grid are critical information for the operation of the grid-connected power conditioning equipments. In such applications, an accurate and fast detection of the phase angle of the utility voltage is essential to assure a correct generation of the reference signals. This paper presents two improved phase-locked-loop (PLL) methods for single-phase grid connected systems. The investigated PLL methods are based on a transport delay method and an inverse Park transformation method. The improvements in the case of using the delay-based PLL are: non-frequency dependent and better filtering of the harmonics. For the other investigated PLL method based on inverse Park transformation the improvement consists of better filtering of the harmonics. Experimental results validate the effectiveness of the two proposed methods.**

***Index Terms* — Phase-Locked-Loop (PLL), single-phase distributed generation system, grid connected power converter.**

I. INTRODUCTION

PHASE, amplitude and frequency of the utility voltage are critical information for the operation of the grid-connected power conditioning and power generating equipments. In such applications, an accurate and fast detection of the phase angle of the utility voltage is essential to assure the correct generation of the reference signals.

The phase-locked loop (PLL) [1], [2] structure is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. The purpose of the PLL in a grid connected system is to synchronize the inverter current angle, θ_{inv}, with the angle of the grid voltage, θ_{grid}, in order to obtain a power factor as close to unity as possible. The angle θ_{inv} is used to calculate the reference current that is compared to the actual output current of the inverter. The main idea in the PLL is that it changes the inverter current frequency, ω_{inv}, if the inverter current and the grid voltage are out of phase. If the inverter current lags the grid voltage the PLL will decrease ω_{inv} until the inverter current is in phase with the grid voltage. On the other hand, if the inverter current leads the grid voltage, ω_{inv} is increased until they are in phase. In order to be able to synchronize θ_{inv} with θ_{grid} it is necessary somehow to measure θ_{grid}. This has been done by detecting the zero crossing on the grid voltage as shown in Fig. 1. Instead of the zero crossing detection method another solution are used in nowadays [3]-[7].

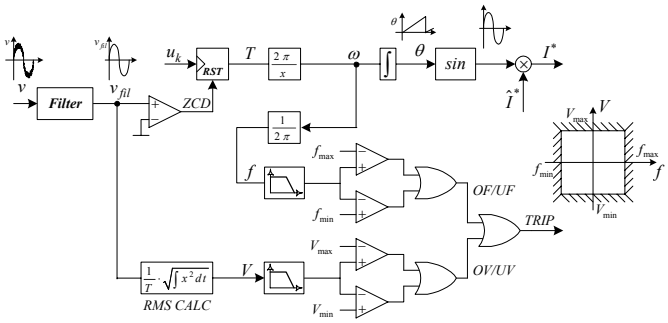

Fig. 1. Zero crossing detection structure including voltage monitoring

Most recently, there has been an increasing interest in Phase-Locked-Loop (PLL) topologies for grid-connected systems [3]. In order to use a PLL method in single-phase systems an artificial orthogonal voltage system should be created [4]. It is well known that in single-phase systems there are less informations than in three-phase systems regarding the grid condition, so more advanced methods should be considered in order to create an orthogonal voltage system [3]-[6].

Also using a PLL structure the grid voltage parameters can be monitored such as grid voltage amplitude and frequency. This grid voltage monitoring is used to ensure that the performances of the investigated methods comply with the standard requirements for operation under common utility distortions such as line notching/harmonics, voltage sags/swells/loss, frequency variations and phase jumps.

This paper presents two different improved methods for single-phase PLL structures.

II. THE SINGLE PHASE PLL STRUCTURE

The general structure of a single-phase PLL is shown in Fig. 2.

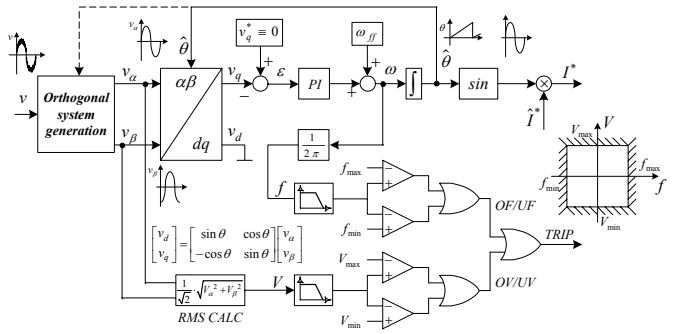

Fig. 2. General structure of a single-phase PLL including voltage monitoring.

An easy way to generate a quadrature signal in a single-phase system is through the use of a transport delay block, which is responsible for introducing a phase shift of 90 degrees with respect to the fundamental frequency of the input signal (grid voltage) [3]. A related method, but more complex is to generate the quadrature signal through the use of Hilbert transformation [5]. Due to its noncausality, it is not practically realizable, but it is possible to be approximated with a high order Finite Impulse Response (FIR) filter. The two mentioned methods are presented in Fig. 3a and Fig. 3b, respectively.

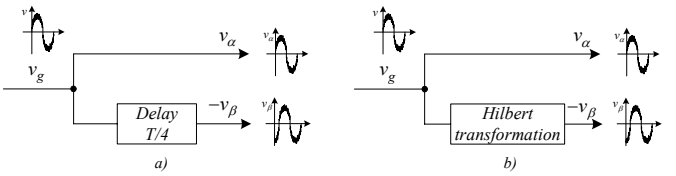

Fig. 3. Orthogonal signal generation based on: a) transport delay, b) Hilbert transformation.

The basic difference of the transport delay method, compared with the Hilbert transformation method is that, all the harmonic content of the input signal is subjected to the same time delay. For the Hilbert transformation method, all the harmonic content is phase-shifted 90 degrees. Therefore, the Hilbert transformation method will not be further investigated in this paper due to its complexity and poor behavior compared with the delay method [3].

The transport delay method is easily implemented through the use of a first-in, first-out (FIFO) buffer, with size set to one-fourth of the number of samples contained in one cycle of the fundamental frequency. Generally speaking, the algorithm is easily implemented and the tuning process does not pose special difficulties. Anyway, the transport delay method has also two drawbacks: it is frequency dependent due to its fixed delay, therefore problems can occur when the grid frequency experience fluctuations, and create an unfiltered orthogonal system.

A different method to generate the orthogonal system is using the inverse Park Transformation, introduced in [4]. The inverse Park method is presented in Fig. 4.

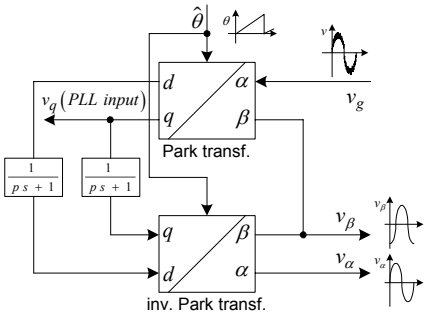

Fig. 4. Orthogonal system generation based on inverse Park transformation.

As it can be seen, a single phase voltage (V_g) and an internally generated signal (V_β) are used as input to a Park transformation block ($\alpha\beta$-dq). V_β is obtained through the use of an inverse Park transformation, where the inputs are the d- and q-axis output of the Park transformation, fed through first order low pass filters (LPF). The two first order lag blocks added to the structure must be adequately tuned in order to guarantee the performance of the single-phase PLL [6]. The inner loop (the β-axis voltage loop) must be fast enough so that the outer loop performs the tracking function with the β-axis voltage stabilized. The stationary frame is seen by the outer loop as if it was obtained from a three phase system and thus the tracking of the "virtual" utility voltage vector can be performed. The tuning of the two first order lag blocks is performed using the following method [6]:

- Set the location of the poles for suitable bandwidth and robustness, considering the continuous variation of this parameters with the phase angle of the input signal;
- Evaluate the disturbance rejection characteristic.

Although the algorithm of the inverse Park transformation is easily implemented, requiring only an inverse Park and two first-order low-pass filters, the tuning of the PI controller and the choice of the time constant of the filters are a more difficult process, as compared with other PLL algorithms. This is due to the presence of the two interdependent nonlinear loops, which make linearization and use of linear system analysis tools more trouble some [3].

III. IMPROVED PLL STRUCTURES

A. Transport delay method

One of the improved single-phase PLL structure methods uses the transport delay block. Due to the fact that this method uses a constant delay in order to generate the quadrature signal of the grid voltage, when the grid frequency experiences fluctuations, the single-phase PLL behavior will be negatively affected. When the grid frequency changes its value, the transport delay block is not able to modify its fixed value and the produced signal will not be in a quadrature with the input signal (V_g). This issue will generate errors in the grid voltage phase angle, frequency and amplitude measurement. The proposed method using the transport delay-based PLL structure is presented in the following.

In order to eliminate this drawback of the transport delay method, a small change in the initial Park transformation is proposed.

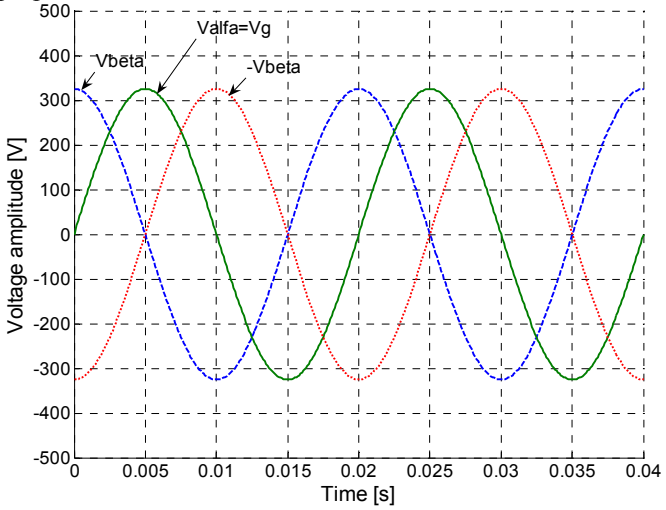

Fig. 5. Orthogonal voltage system.

Fig. 5 shows an orthogonal voltage system where the grid voltage represents the α-signal. The reference frames considered in the transformations is depicted in Fig. 6. Eq. (1) shows the direct Park transformation utilized in Fig. 2.

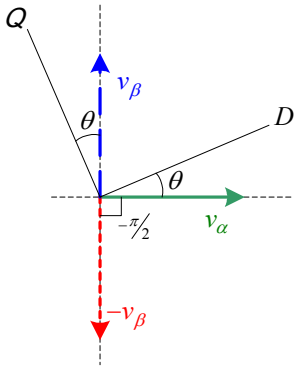

Fig. 6. Reference frames of the orthogonal voltage system.

$$\begin{cases} v_d = v_\alpha \cdot \sin\hat{\theta} + v_\beta \cdot \cos\hat{\theta} \\ v_q = -v_\alpha \cdot \cos\hat{\theta} + v_\beta \cdot \sin\hat{\theta} \end{cases} \quad (1)$$

- where $\hat{\theta}$ represents the estimated grid voltage angle provided by the PLL structure.

When a transport delay block is used, a quadrature signal of the input is created. If the grid voltage represents the α-signal, the obtained quadrature signal provided by the transport delay block will be $-v_\beta$ as presented in Fig. 5 and Fig. 6. The orthogonal voltage system created by using transport delay method is presented as follows:

$$\begin{cases} \sin(\omega_{50}\cdot t) \rightarrow \boxed{delay\ T_{50}/4} \rightarrow \sin\left(\omega_{50}\cdot t - T_{50}/4\right) = -\cos(\omega_{50}\cdot t) \\ v_\alpha = V_g \cdot \sin\theta \\ -v_\beta = V_g \cdot \sin(\theta - T_{50}/2) \end{cases} \quad (2)$$

Therefore, the transport delay block provides a quadrature signal equal with $-v_\beta$ instead of v_β, which should be taken into consideration when the Park transformation is used.

Thus, (1) will become as presented in (3):

$$\begin{cases} v_d = v_\alpha \cdot \sin\hat{\theta} - (-v_\beta) \cdot \cos\hat{\theta} \\ v_q = -v_\alpha \cdot \cos\hat{\theta} - (-v_\beta) \cdot \sin\hat{\theta} \end{cases} \quad (3)$$

Substituting v_α and $-v_\beta$ from (2) into (3) results in:

$$\begin{cases} v_d = V_g \cdot \sin\theta \cdot \sin\hat{\theta} - V_g \cdot \sin(\theta - T_{50}/4) \cdot \cos\hat{\theta} \\ v_q = -V_g \cdot \sin\theta \cdot \cos\hat{\theta} - V_g \cdot \sin(\theta - T_{50}/4) \cdot \sin\hat{\theta} \end{cases} \quad (4)$$

The second term of (4) (v_q), used in the control loop of the PLL structure as input, becomes as follows:

$$v_q = V_g \cdot \left[-\sin(\omega_{50}\cdot t) \cdot \cos\widehat{(\omega_{50}\cdot t)} - \sin\left(\omega_{50}\cdot t - T_{50}/4\right) \cdot \sin\widehat{(\omega_{50}\cdot t)} \right] \quad (5)$$

Substituting $\sin\left(\omega_{50}\cdot t - T_{50}/4\right) = -\cos(\omega_{50}\cdot t)$ (5) will become:

$$v_q = V_g \cdot \underbrace{\left[\sin\widehat{(\omega_{50}\cdot t)} \cdot \cos(\omega_{50}\cdot t) - \sin(\omega_{50}\cdot t) \cdot \cos\widehat{(\omega_{50}\cdot t)} \right]}_{\equiv 0,\ when\ \hat{\theta}=\theta} \quad (6)$$

When the frequency changes its value from ω_{50} to ω_n, the constant delay will generate a phase shift error (φ_{er}) in the quadrature signal as presented in (5):

$$\sin(\omega_n\cdot t) \rightarrow \boxed{delay\ T_{50}/4} \rightarrow \sin\left(\omega_n\cdot t - T_{50}/4 + \varphi_{er}\right) \quad (7)$$

If the grid frequency changes its value from ω_{50} to ω_n, (5) becomes:

$$v_q = V_g \cdot \underbrace{\left[-\sin(\omega_n\cdot t) \cdot \cos\widehat{(\omega_n\cdot t)} - \sin\left(\omega_n\cdot t - T_{50}/4 + \varphi_{er}\right) \cdot \sin\widehat{(\omega_n\cdot t)} \right]}_{\neq 0,\ when\ \hat{\theta}=\theta} \quad (8)$$

In order to eliminate the errors introduced by φ_{er}, a change in the Park transformation is proposed. The change consists in the substitution of $\cos\hat{\theta}$ of the Park transformation presented in (1) with the quadrature signal of $\sin\hat{\theta}$ using the same transport delay block as in case when $-v_\beta$ is created:

$$\sin\widehat{(\omega_n\cdot t)} \rightarrow \boxed{delay\ T_{50}/4} \rightarrow \sin\left(\widehat{\omega_n\cdot t} - T_{50}/4 + \varphi_{er}\right) = -\cos\widehat{(\omega_n\cdot t)} \quad (9)$$

resulting:

$$\cos\widehat{(\omega_n\cdot t)} = -\sin\left(\widehat{\omega_n\cdot t} - T_{50}/4 + \varphi_{er}\right) \quad (10)$$

The substitution presented in (10) will produce the same phase shift error (φ_{er}) as in the case of generating $-v_\beta$ using the transport delay block.

Using (10) in (8) results in:

$$v_q = V_g \cdot \underbrace{\left[\sin\left(\widehat{\omega_n\cdot t} - T_{50}/4 + \varphi_{er}\right) \cdot \sin(\omega_n\cdot t) - \sin\left(\omega_n\cdot t - T_{50}/4 + \varphi_{er}\right) \cdot \sin\widehat{(\omega_n\cdot t)} \right]}_{\equiv 0,\ when\ \hat{\theta}=\theta} \quad (11)$$

As it can be seen from (11), if the grid frequency changes

its value from ω_{50} to ω_n, the v_q term will not be affected (at $\hat{\theta} = \theta$).

Another improvement for the transport delay method consists in using a first-order LPF in order to get a clean v_q as presented in Fig. 7. The dynamics of the PLL will be slightly affected in this case, while the harmonic content from v_q will decrease considerably.

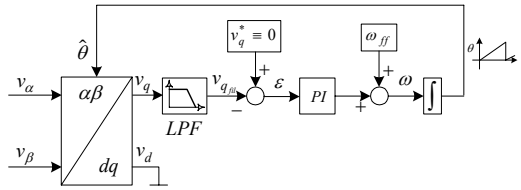

Fig. 7. PLL with v_q filtering using a first-order low-pass filter.

B. Park transformation method

As it can be seen from Fig. 4, the v_q output of the Park transformation is used directly as input for the PLL structure to obtain phase and frequency information of the input signal (grid voltage) [3]. In the case of high harmonic content in the grid voltage, the v_q output of the Park transformation will be affected due to the fact that one of the two inputs of the Park transformation ($v_\alpha = v_g$) is not filtered.

In order to avoid the harmonic propagation into the PLL control loop a new Park transformation can be used, as presented in Fig. 8. The inputs of this new Park transformation will be the outputs (v_α and v_β) of the inverse Park transformation. Therefore, instead of using the v_q signal directly as input for the PLL control loop (see Fig. 4), a new Park transformation using two clean outputs (v_α and v_β) of the inverse Park transformation is used (see Fig. 8). The harmonic content from v_q will be significantly decreased in this case, while the dynamic of the PLL will be slightly affected.

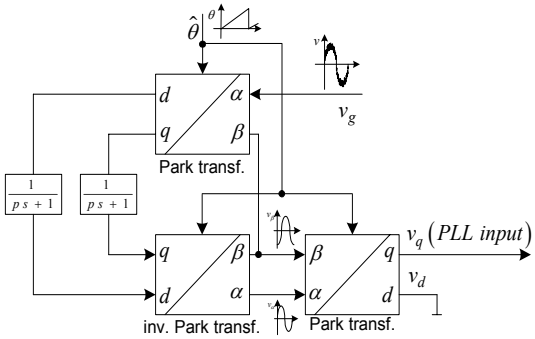

Fig. 8. Improved Park transformation PLL method.

IV. Experimental Results

The single-phase PLL topologies were implemented in a dSPACE DS1103 based system [7]. In order to test the PLL structures and to observe their behavior under different grid conditions, an experimental system connected to a grid simulator (California Instruments) has been used.

A. Transport delay method

Three types of disturbances were used to evaluate the behavior of the transport delay based PLL.

The parameters of the PLL structure have been set as follows: - settling time t_{set}= 0.05 seconds and damping factor ξ=1. The sampling frequency was equal to 10 kHz.

A frequency sweep from 50 to 51 Hz was created, in order to test the improved transport delay based PLL at frequency variations. Fig. 9 presents the estimated grid frequency of a PLL structure using the classical delay method. The estimated grid frequency of the improved delay method, presented in § III.A, is shown in Fig. 10. It can be seen that the improved method is not frequency dependent as the classical method is.

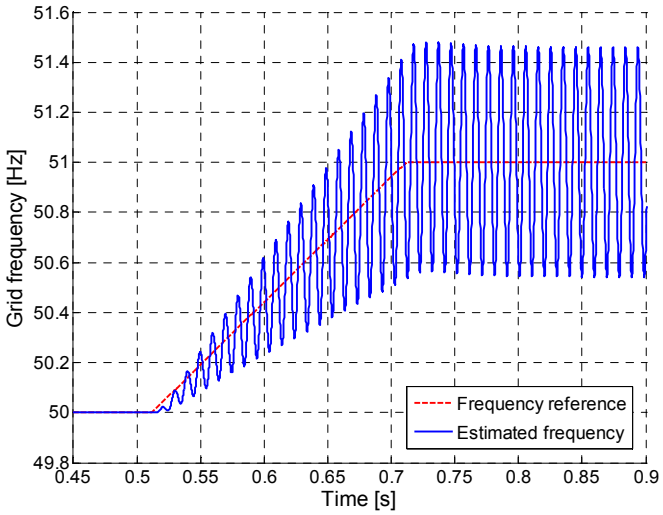

Fig. 9. Frequency sweep response of the classical delay based PLL.

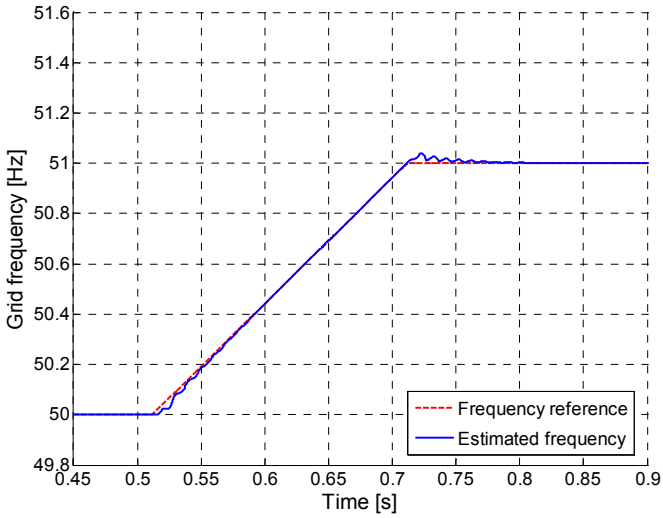

Fig. 10. Frequency sweep response of the improved delay based PLL.

The behavior of the classical delay and improved delay methods under a sudden phase jump of 45 degrees is presented in Fig. 11. A non significant difference between the responses of the two methods can be observed.

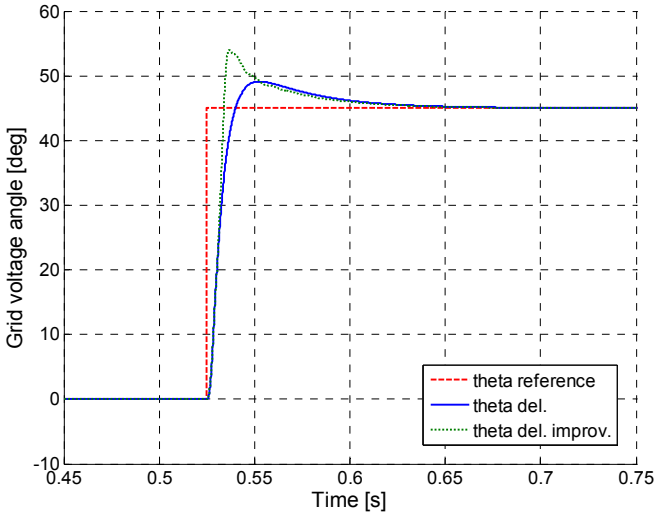

Fig. 11. Operation of the delay based PLL under a 45° phase angle jump.

Fig. 12 and Fig. 13 illustrate the behavior of the improved delay based PLL (without and with LPF on v_q) under a frequency step from 50 to 51 Hz. An abnormal high harmonic content of the input voltage signal (THD=12%) was also considered in these measurements.

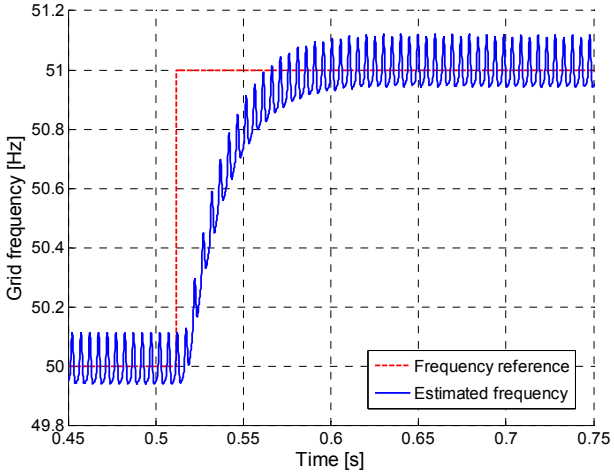

Fig. 12. Estimated frequency by the delay based PLL without LPF.

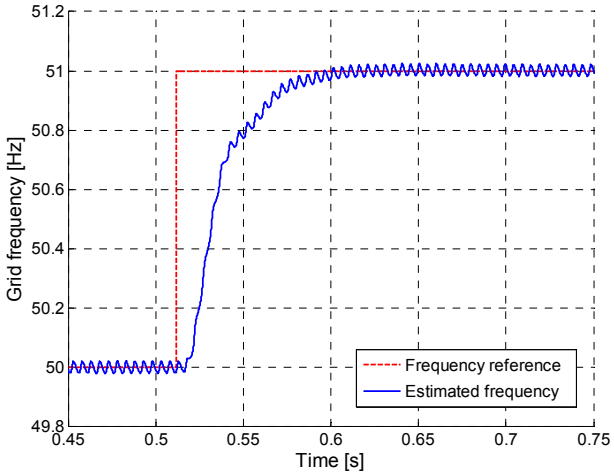

Fig. 13. Estimated frequency by the delay based PLL with LPF.

The estimated grid frequency provided by the PLL structure was filtered in the both cases, using another first-order LPF with a cut-off frequency equal to 6 Hz.

A clean estimated grid frequency is obtained when a LPF is used on v_q, as shown in Fig. 13. The cut-off frequency of the LPF was set to 70 Hz. The ripple in the phase angle of the improved delay based PLL is decreased and the response time is preserved, as presented in Fig. 14.

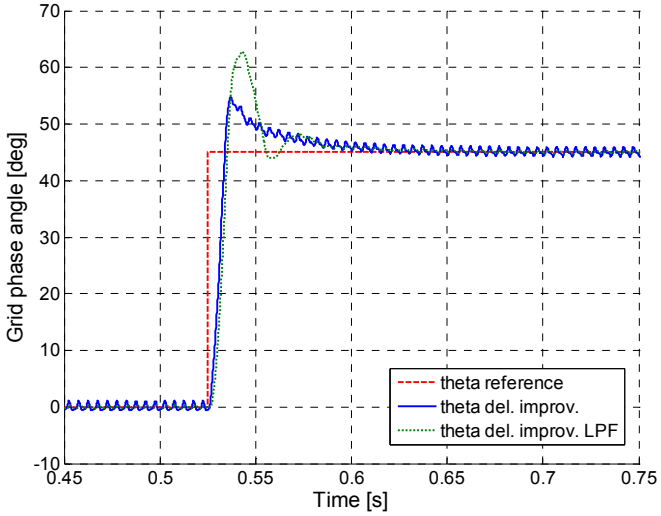

Fig. 14. Operation of the improved delay based PLL under a 45° phase angle jump, with and without a LPF.

B. Park transformation method

Fig. 15 and Fig. 16 illustrate the behavior of the inverse Park based PLL (without and with a new Park transformation as presented in § III.B) under a frequency step from 50 to 51 Hz. An abnormal high harmonic content of the input voltage signal (THD=12%) was also considered in these measurements.

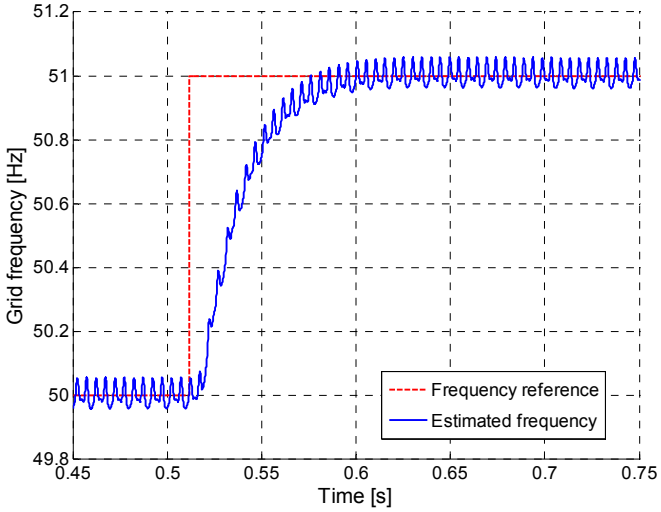

Fig. 15. Estimated frequency by the inverse Park based PLL.

The estimated grid frequency provided by the inverse Park based PLL was filtered in the both cases, using a first-order LPF with a cut-off frequency equal to 6 Hz.

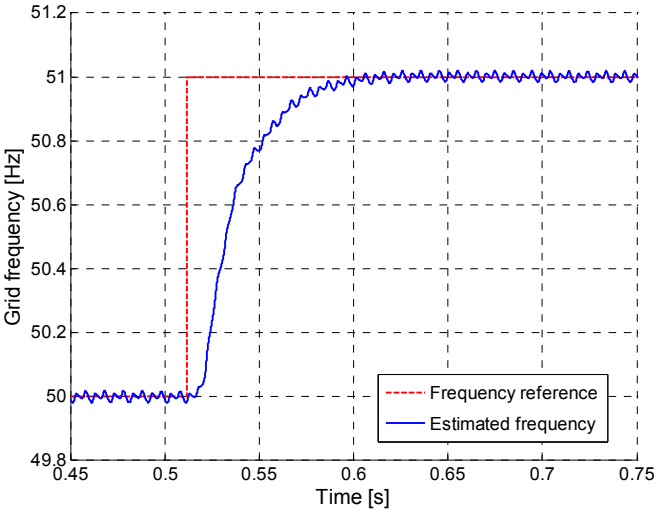

Fig. 16. Estimated frequency by the improved inverse Park based PLL.

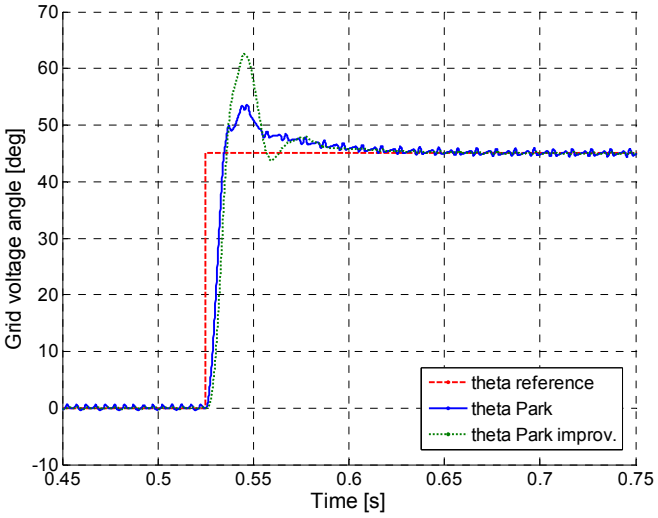

Fig. 17. Operation of the inverse Park based PLL under a 45° phase angle jump.

The behavior of the inverse Park based PLL (without and with a new Park transformation) under a sudden phase jump of 45 degrees is presented in Fig. 17. The ripple in the phase angle of the improved inverse Park based PLL is decreased and the response time is preserved.

V. Conclusion

In this paper two improved PLL methods for single-phase systems have been presented. The investigated PLL methods are based on transport delay block and inverse Park transformation.

The improvements in the case of using the delay-based PLL are: non frequency dependent and better filtering of the harmonics.

For the inverse Park transformation based PLL the improvement consists of better filtering of the orthogonal voltage system.

Experimental results validate the effectiveness of the proposed methods.

References

[1] S.K. Chung, "*Phase-Locked Loop for Grid-Connected Three-Phase power conversion systems*", IEE Proc. – Electr. Power Appl., Vol. 147, No. 3, 2000, pp. 213-219.

[2] G. Hsieh, and J.C. Hung, "Phase-locked loop techniques – a survey," *IEEE Trans. on Industrial Electronics*, 1996, vol. 43, no. 6, pp. 609-615.

[3] S.M. Silva, B.M. Lopes, B.C. Filho, R.P. Campana and W.C. Boaventura, "*Performance evaluation of PLL algorithms for single-phase grid-connected systems*", Proc.of IAS'04, vol. 4, pp. 2259 - 2263.

[4] S.M. Silva, M. Sidelmo, L.N. Arruda and B.C. Filho, "*Wide Bandwidth Single and Three-Phase PLL Structures for Utility Connected Systems*", Proc. of EPE'01, pp. 1660-1663.

[5] M. Saitou, N. Matsui and T. Shimizu, "*A Control Strategy of Single-phase Active Filter using a Novel d-q Transformation*", proc. of IAS'03, vol. 2, pp.1222-1227.

[6] L.N. Arruda, S.M. Silva and B.C. Filho, "*PLL Structures for Utility Connected Systems*", Proc. of IAS'04, vol. 4, pp. 2655–2660.

[7] M. Ciobotaru, R. Teodorescu and F. Blaabjerg, "*Control of Single-Stage Single-Phase PV Inverter*", Proc. of EPE'05, ISBN: 90-75815-08-5.