PLL Structures for Utility Connected Systems

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Abstract – **This paper presents a detailed analysis of PLL structures for utility connected systems. The three-phase PLL (Phase-Locked Loop) structure capable of fast tracking the utility voltage vector is studied. A single-phase PLL structure, derived from the three-phase PLL topology, is discussed and its behavior under distorted utility conditions is analyzed. Additionally, the conventional zero-crossing PLL is studied and an alternative implementation for this PLL is proposed in order to improve its dynamic behavior. Simulation and experimental results from a DSP-based system are included to support the theoretical analysis.**

I. INTRODUCTION

The phase angle of the utility voltage vector is a basic information for an increasing number of grid-connected power conditioning equipments, such as AC/DC converters, uninterruptible power systems (UPS), series voltage compensators and the emerging distributed generation systems. In such applications, an accurate and fast detection of the phase angle of the utility voltage is essential to assure the correct generation of the reference signals. Thus, phase-locked loop (PLL) topologies must handle distorted utility voltages if they are intended to applications that require the tracking of the utility voltage vector [1-5].

Most recently, there have been an increasing interest in PLL topologies for grid-connected systems [1-5]. The three-phase PLL discussed in [4] uses a synchronous reference frame (SRF) to detect the phase angle, the frequency and the amplitude of the utility voltage vector. The phase detecting method discussed in [1] also deals with the three-phase PLL topology. A better performance of the SRF PLL under unbalanced utility voltages is achieved by separating the positive and negative sequences present in these voltages and by feeding back only the positive sequence. The PLL structure introduced in [2] utilizes a weighted least-square method as an alternative way to calculate the positive and negative sequences of the utility voltages and thus improve the tracking performance of the three-phase PLL topology. An important issue in this area that has not been sufficiently explored is a methodology for tuning the PI or lead-lag controller used in the PLL topologies.

This paper presents a description of the three-phase PLL topology along with a methodology for tuning its feedback gains. The dynamic behavior of this topology under distorted utility conditions is used as a tuning criterion. Additionally, a single-phase PLL structure, derived from the three-phase topology, and the zero-crossing PLL structure are also considered for operation under utility disturbances. Simulation and experimental results obtained from a DSP-based system are presented to support the theoretical analysis.

II. THE THREE-PHASE PLL STRUCTURE

The three-phase PLL topology is illustrated in Fig. 1 [4]. In this PLL, the phase angle is detected by synchronizing the PLL rotating reference frame and the utility voltage vector [3-5]. Setting the direct axis reference voltage (V_d^*) to zero results in the lock in of the PLL output on the phase angle of the utility voltage vector. In addition, the instantaneous frequency and amplitude of the voltage vector are also determined. The feedforward frequency command ($_{ff}$) is introduced to improve the overall tracking performance of the PLL.

The tuning of the feedback gains requires the determination of an equivalent linear model, shown in Fig. 2. From this small signal model, one can derive the state space representation of the three-phase PLL topology (1).

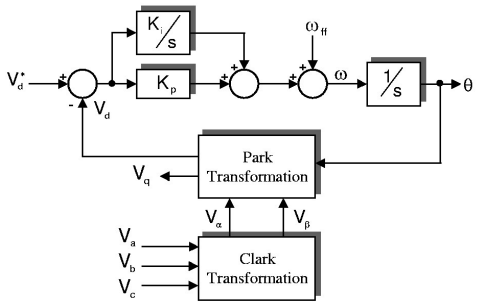

Fig. 1. Three-phase PLL structure.

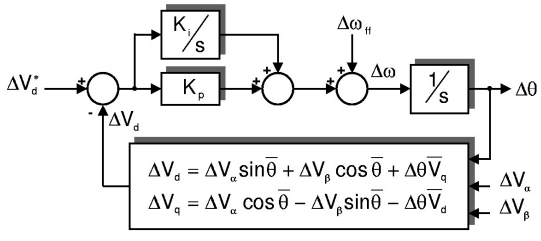

Fig. 2. Small signal model of the three-phase PLL structure.

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$$\frac{d}{dt}\begin{matrix} dt \\ \\ \end{matrix} = \begin{matrix} 0 & 1 \\ K_i\overline{V}_q & K_p\overline{V}_q \end{matrix} + \begin{matrix} V\ dt \\ V\ dt \\ V \\ V \end{matrix} + \begin{matrix} 0 & 0 & 0 & 0 \\ K_i\sin^{-} & K_i\cos^{-} & K_p\sin^{-} & K_p\cos^{-} \end{matrix} \quad (1)$$

Following the determination of an equivalent linear model, it is necessary to adopt some criteria in order to impose an adequate dynamic behavior on the three-phase PLL topology:

By imposing an acceptable distance between the fastest pole and the sampling frequency of the DSP, one can guarantee the affective application of the PLL tracking commands.

A better robustness of the three-phase PLL is achieved by imposing an adequate distance between closed-loop poles.

The behavior of the PLL under distorted utility conditions is determined from the analysis of the dynamic stiffness of this topology, as stated in (2). The closed-loop disturbance rejection characteristic of the three-phase PLL depends on the intended application. In systems where the fundamental component of the utility voltage vector must be tracked, it is necessary to elevate the dynamic stiffness figures in order to better reject undesired harmonic components. On the other hand, there are systems where the distortions present in the utility voltages might be known (e.g. for compensation actions) and thus the dynamic stiffness characteristics has to be shaped accordingly.

$$\left|\frac{V}{\quad}\right| = \frac{s^2 + sK_p\overline{V}_q + K_i\overline{V}_q}{sK_p\sin} \quad (2)$$

Fig. 3 illustrates the influence of the parameters of the PLL topology on the dynamic stiffness characteristic. As shown in Table I (the gains were set for a 220V, 60Hz system and a DSP sampling frequency of 10kHz was used), there must be a trade-off between the dynamic stiffness and the robustness of the systems. Higher integral gains result in a better rejection characteristic (Fig. 3) in the lower frequency region but the robustness of the system is deteriorated as the poles become closer (Table I). Larger bandwidth is achieved for higher proportional gains (Table I) at the expense of the deterioration of the overall dynamic stiffness characteristic (Fig. 3). Once again, the tuning of the PLL depends on the intended application.

It is remarkable the dependence of the dynamic stiffness, and thus the pole locations, on the instantaneous value of the phase angle of the input voltage signal. As illustrated in Fig. 4 (220V/60Hz system; K_i=40000; K_p=50), the dynamic stiffness curve is continuously varied during the operation of the PLL.

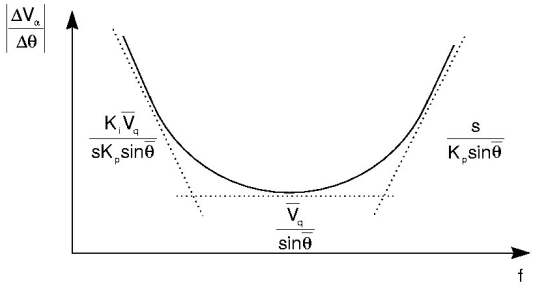

Fig. 3. Qualitative dynamic stiffness curve of the three-phase PLL topology.

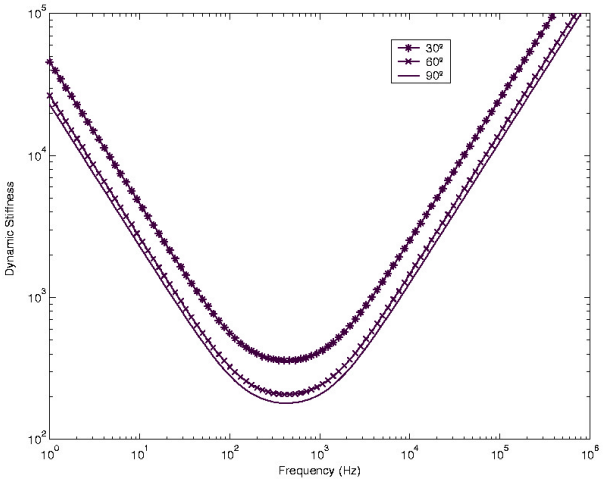

Fig. 4. Influence of the phase angle over the dynamic stiffness.

TABLE I
LOCATION OF THE POLES OF THE THREE-PHASE PLL STRUCTURE (= 60º)

K_p	K_i	Poles (Hz)
50	20000	(68;1366)
	30000	(103;1330)
	40000	(141;1291)
	50000	(182;1250)
	60000	(227;1206)
30	40000	(382;477)
40		(191;955)
50		(141;1291)
60		(114;1605)
70		(96;1910)

It should be noted that the lowest value of the dynamic stiffness curve is limited to the value of the amplitude of the voltage vector (V_p=180V). This limit can be improved by the replacement of the PI controller for a lead-lag one (3). The introduction of the lead-lag controller results in a new form for PLL dynamic stiffness characteristic (4). Despite the possibility of imposing a displacement in the dynamic stiffness characteristic (through the parameter b), it is important to note that practical problems can result from the presence of a derivative term in the controller.

$$F(s) = \frac{K(s+a)}{(s+b)} \quad (3)$$

$$\left|\frac{V}{\quad}\right| = \frac{s^2 + s\left(b + K\bar{V}_q\right) + Ka\bar{V}_q}{sKsin} \tag{4}$$

A. Experimental Results

The three-phase PLL topology was implemented in a fixed-point Analog Devices DSP-based system (ADMC401), with 12-bit A/D converter and 16-bit arithmetic registers. The sampling frequency of the DSP was set to 10kHz and the closed-loop poles were set to 175Hz and 1.76kHz. The tuning of the PLL was done based on an application that requires tracking of the fundamental component of the utility voltage vector. Fig. 5 shows the phase of the utility voltage vector entering the DSP (CH1) and the PLL output (CH2). Despite the abnormal distorted conditions imposed to the utility voltages (the total harmonic distortion – THD – of the input signal was set to 10%), the PLL output is able to attenuate the undesired harmonic components, as illustrated in Fig. 6. The behavior of the PLL under different levels of angle jumps was also analyzed. As shown in Fig. 7, an angle jump of 30º in the input signal is quickly tracked by the PLL in 1ms, approximately.

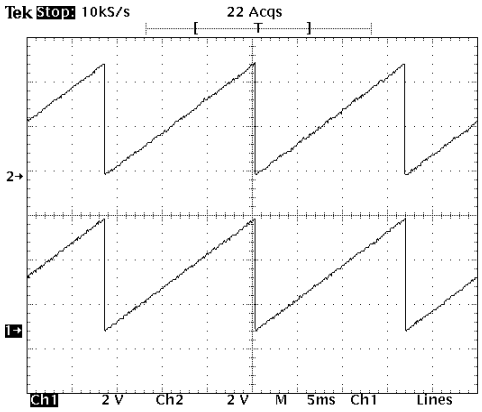

Fig. 5. Phase of the input voltage vector (CH1) and PLL output (CH2).

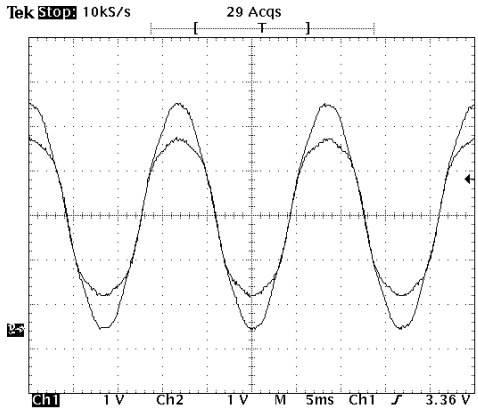

Fig. 6. Input voltage and reference signal generated by the PLL.

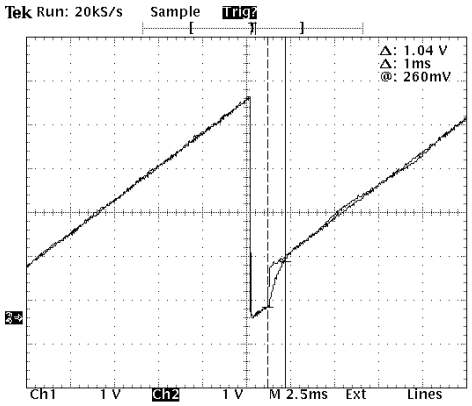

Fig. 7. Input and output of the PLL for a 30º angle jump.

III. THE SINGLE-PHASE PLL STRUCTURE

The single-phase PLL structure illustrated in Fig. 8 is derived from the three-phase SRF topology [3][5]. It is based on the emulation of a balanced three-phase system: the -axis voltage of the stationary frame is made equal to the single-phase voltage of the utility, while the -axis voltage is internally synthesized by the PLL through an inverse Park Transformation block. The three first order lag blocks added to the structure must be adequately tuned in order to guarantee the performance of the single-phase PLL. The inner loop (the -axis voltage loop) must be fast enough so that the outer loop performs the tracking function with the -axis voltage stabilized. The stationary frame is seen by the outer loop as if it were obtained from a three-phase system and thus the tracking of the "virtual" utility voltage vector can be performed.

The small-signal model of the single-phase PLL is shown in Fig. 9. The tuning of the lead-lag controller gains is performed using the same methodology already discussed for the three-phase topology:

Set the location of the poles for suitable bandwidth and robustness, considering the continuous variation of this parameters with the phase angle of the input signal;

Evaluate the disturbance rejection characteristic.

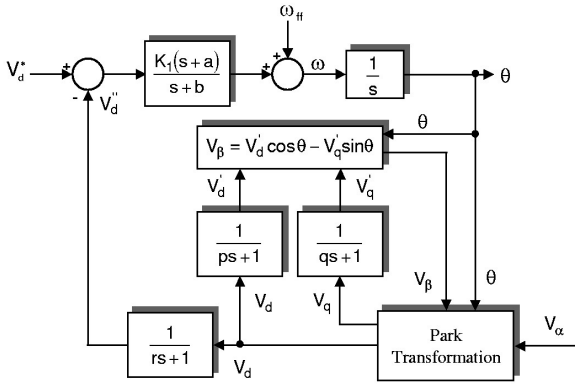

Fig. 8. Single-phase PLL topology.

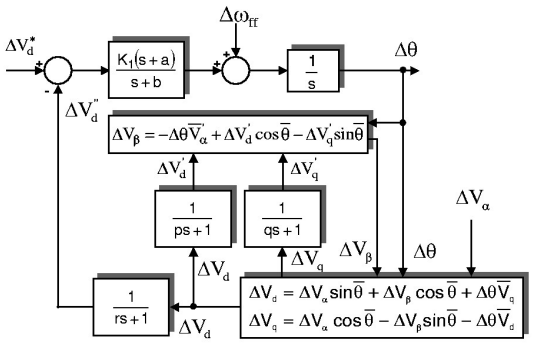

Fig. 9. Small-signal model of the single-phase PLL topology.

A. Experimental Results

The single-phase PLL topology was implemented in the ADMC401 DSP based system. Aiming at power electronics applications such as rectifiers with input power factor control, active filters and distributed generation systems, three types of disturbances were used to evaluate the behavior of the PLL:

Sudden phase jump: Fig. 10 shows the output of the PLL following the application of a 30º increment to the input signal phase angle. The single-phase PLL was able to track the input signal in less than one cycle.

Voltage sag and harmonics: Fig. 11 and Fig. 12 illustrate the behavior of the single-phase PLL under a voltage sag of 0.6pu and a sudden phase jump of +10º in the input voltage signal. An abnormal high harmonic content of the input voltage signal (THD = 15%) was also considered in these measurements. Due to the tuning of the controller gains and the trade-off between the bandwidth and the dynamic stiffness, the PLL was able to track the input signal and, additionally, attenuate the harmonic content in the PLL output (1.8%), as illustrated in Fig. 13.

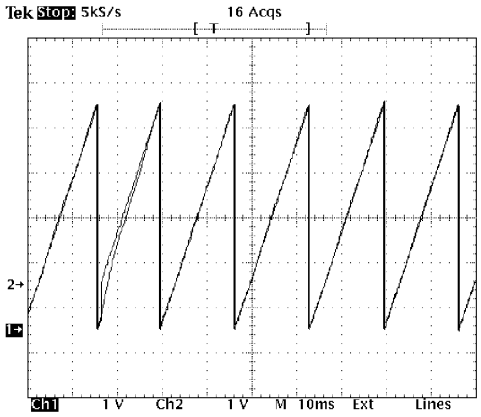

Fig. 10. Operation of the PLL under a 30º phase angle jump.

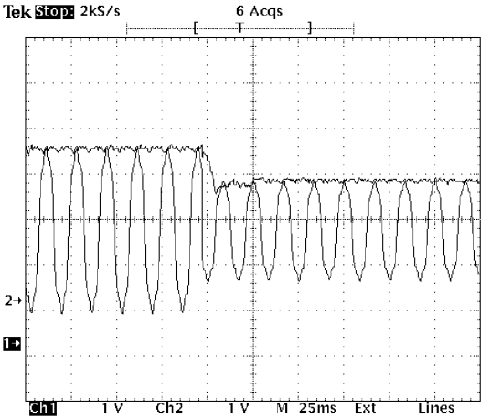

Fig. 11. Operation of the PLL under a 0.6pu voltage sag (THD of the input signal = 15%).

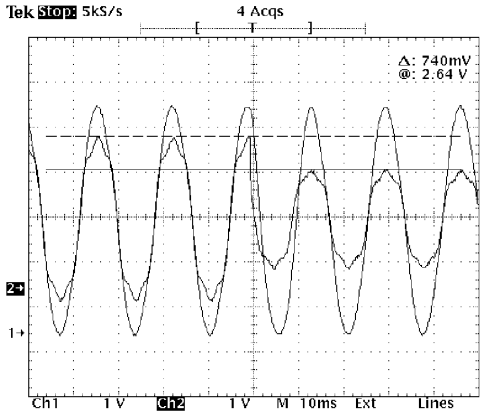

Fig. 12. Operation of the PLL under a 0.6pu voltage sag and a phase angle jump of 10º (THD of the input signal = 15%).

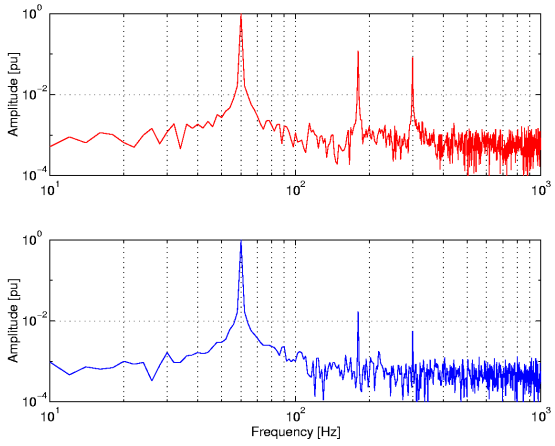

Fig. 13. Frequency spectrum of the input voltage signal applied to the PLL (THD = 15%) and the spectrum of output signal (THD = 1.8%).

IV. THE ZERO CROSSING PLL STRUCTURE

One of the most used PLL structures is constructed with discrete electronic components and is based on a phase detec-

tor, a low-pass filter and a voltage-controlled oscillator (VCO), as shown in Fig. 14. This topology can be classified as zero-crossing structure in which the detection of phase and frequency is based on the zero crossing points of the input signal. The square wave generated from a sample of the utility voltage is used as one of the inputs of the phase detector, implemented via a XOR (exclusive-or) gate. The output of the phase detector is filtered through a low-pass filter in order to generate a DC voltage signal, which act as a reference voltage to the VCO. The center frequency of the VCO, the number of bits of the counter and of the memory address bus are related with the desired phase resolution of the PLL output signal. The output of the VCO is used as a clock signal for the counter, which generate the addresses for the memory device. The most significant bit of the counter is then feedback through the second input of the phase detector, allowing the synchronization of the PLL output with the input signal. A digital-to-analog (D/A) converter connected to the memory device is used to generate the analog sinusoidal voltage, which after a low-pass filtering stage is the output of the PLL. For a input signal of 60Hz and a 12-bits counter it is possible to obtain a phase resolution for the PLL given in (5). In this case, the VCO center frequency should be chosen as indicated in (6).

$$r = \frac{2}{2^{12}} = 1.53 \quad 10^{\ 3}\,\text{rad} \tag{5}$$

$$f_{VCO} = 2^{12} \quad 60 = 245.76\text{kHz} \tag{6}$$

As recommended by the manufacturer [8], the filter in the phase-detector output should be designed to cut off all frequencies above twice the input signal frequency. In the case of a first order low-pass filter, its cutoff frequency should be approximately 12Hz, for an attenuation of –20dB in the phase detector output signal, considering a system with 60Hz. This design practice, associated with the phase detection on the zero-crossing points lead to very poor dynamic response for this PLL structure, as will be shown later. In this study, the cutoff frequency of the VCO input filter was varied in a wide frequency range, in order to improve the dynamic response of the PLL.

A. Experimental Results

The zero-crossing PLL structure was implemented and tested in order to evaluate its performance under utility voltage disturbances. It was used a CD4046 with the XOR gate (Comparator I). The optional phase comparator -Comparator II- of this chip has a very poor dynamic response and was not considered in this study. The low-pass filter was designed with a cutoff frequency equal to 12Hz, to give a maximum VCO input ripple of 0.3V, as suggested by the manufacturer [8]. The VCO center frequency was set to 245.76kHz and a 12-bit counter was introduced in the feedback path.

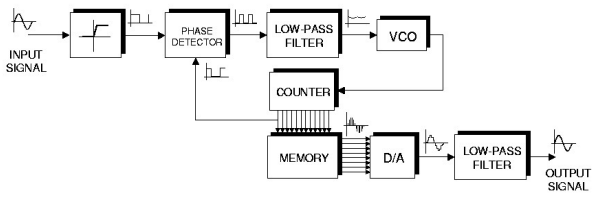

Fig. 14. Zero-crossing PLL topology.

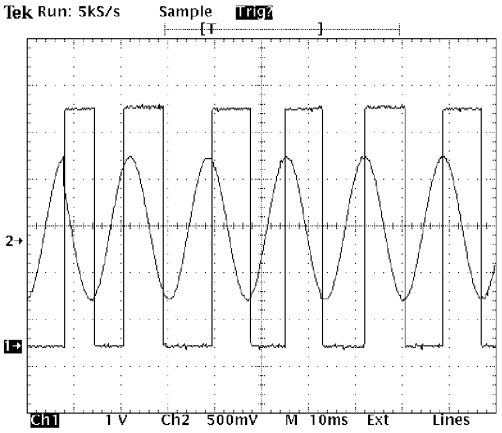

Fig. 15. Zero-crossing PLL response to a 30º phase angle jump (with low-pass filter).

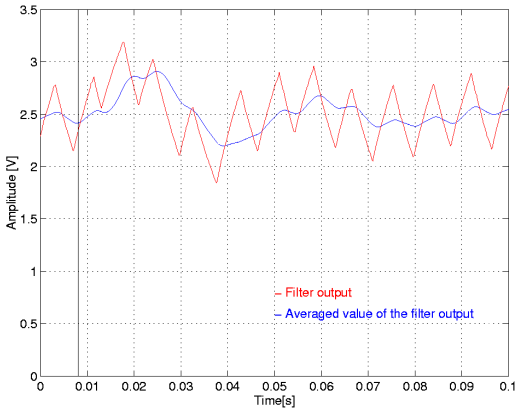

Fig. 16. Oscillation of the VCO low-pass filter output for a 30º phase angle jump.

Fig. 15 shows the input (sine wave) and the most significant bit of the counter (square wave) signals of the PLL for a phase angle jump of 30º. Fig. 16 shows the low-pass filter output and its cycle mean plot for the same situation. As it can be seen, after a sudden phase angle jump, this PLL presents an underdamped response with a settling time of approximately 80ms.

From Figs. 15 and 16, it can be seen that the zero-crossing PLL structure with the low-pass filtering stage has a poor dynamic response. Therefore, its application in utility connected systems must be considered carefully, since disturbances in the utility voltage with phase angle jump can introduce large errors with duration as long as 80ms in the PLL output.

As mentioned before, the PLL operation was evaluated under various cutoff frequencies for the VCO input filter. It was experimentally verified that the VCO is capable of a stable operation even when the output of the phase detector is directly used as the VCO input voltage, without any filtering stage. This alternative implementation significantly improves the dynamic response of the zero-crossing PLL, as shown in Fig. 17.

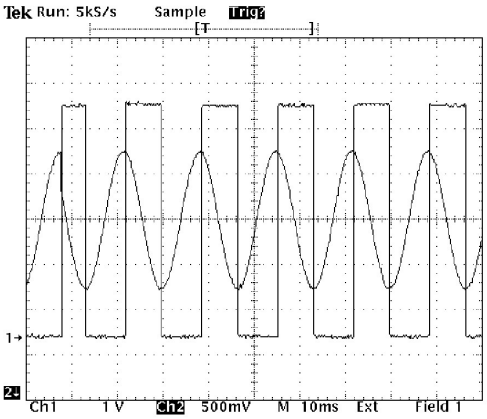

Fig. 17. Zero-crossing PLL response to a 30º phase angle jump (without low-pass filter).

V. CONCLUSIONS

Three different PLL topologies were analyzed in this paper. Issues like bandwidth, robustness and disturbance rejection were focused as tuning and performance criteria. Some characteristics in each of these PLL topologies must be stressed:

The three-phase PLL topology can be adequately tuned in order to give fast tracking response and high disturbance rejection, which can be valuable in many applications. The tuning flexibility of this toplogy permits its use in a wide range of appications. Additional feature of this three-phase PLL topology is the availabitity of the instantaneous values of frequency and amplitude of the utility voltage vector. Further studies must be done in order to evaluate the behavior of this structure under unbalanced conditions.

The single-phase SRF PLL topology showed adequate performance under the tested conditions. As in the prior PLL topology, the instantaneous information of frequency and amplitude of the utility voltage constitutes an additional feature that can be valuable in some applications. The added complexity of this single-phase topology must be also taken into consideration.

The simplicity of the zero-crossing topology is one of its remarkable characteristics. Additionally, the immunity of this structure to harmonics in the input signal can be a very welcome feature in many applications. The dynamic response of the zero-crossing PLL can be improved by elimination of the low-pass filter. Further study is required in this latter alternative.

The different characteristics of the analyzed PLL topologies can be adequately used to fit the requirements of many applications. The tuning criteria and the knowledge of the intended application will determine the utilized structure.

ACKNOWLEDGMENT

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